SEMICONDUCTOR DEVICE CARRYING A PLURALITY OF CIRCUITS

CROSS REFERENCES TO RELATED APPLICATIONS

The present invention claims priority to priority

5   document no. 2001-036757 filed in Japan on Feb. 14, 2001, and

incorporated by reference herein.

BACKGROUND OF THE INVENTION

1.   Field of the Invention

10   The present invention relates to a semiconductor device

that has a plurality of circuits mounted on one chip and each

of the circuits having the same or different function.

2.   Description of the Related Art

As shown in Fig. 5, a semiconductor chip 20 forming part

15   of a semiconductor device is broadly divided into an active

region 21 which is a region for embodying functions as a circuit,

and an I/O (Input/Output) region 23 provided with input

terminals and output terminals required for interfacing the

circuit with an external circuit.

20   The I/O region 23 is formed in the periphery of the

semiconductor chip 20, where a plurality of input/output pads

22 are provided as electrodes for connecting lead-out terminals

for an LSI (Large Scale Integration) with the circuit inside

the semiconductor chip through bonding wires.

25   Each of the input/output pads 22 is typically shaped

to have a square with a side of approximately 100 im. Due

to limitations of mechanical accuracy of a bonding apparatus

for use in a wire bonding process, it is difficult to

significantly reduce the input/output pads 22 in size. Thus,

30   when the required number of input/output pads 22 are arranged

in the periphery of the rectangular chip 20 as shown in Fig.

5, the minimum chip size is accordingly determined

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In the chip size thus determined, the active region 21 surrounded by the I/O region 23 is a region where circuits can be actually placed. When circuits designed to fit in the active region 21 is placed, the circuits are formed over the entire active region 21.

With an increasingly miniaturized LSI, a higher speed processing ability, and realization of an extremely large-scale integrated circuit in a very limited area on a chip, however, the overall active region 21 may not be filled with circuits. In this case, the active region 21 includes an no-patterned region which has no circuit mounted therein. An no-patterned region may also occur for circuits that involve relatively simple signal processing and uses a small number of gates.

On the other hand, the size of the active region 21 is inevitably determined by the number of the input/output pads 22 and the size thereof, i.e. pad size. Since improvement in mechanical accuracy of a bonding apparatus does not catch up with improvement in integration degree, it is impossible to reduce the size of the active region 21 according to the scale of the mounted circuits.

For circuits that do not require high speed processing, occurrence of an no-patterned region can be avoided by lowering its integration degree. For circuits that require high speed processing, however, a higher integration degree (miniaturization) is needed, and in this case, design must be performed in preparation for occurrence of an no-patterned region. In addition, when an no-patterned region occurs, a problem of much waste arises since the no-patterned region cannot be effectively utilized.

In this manner, in a conventional LSI, since the minimum chip size is inevitably determined by the number and size of

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the input/output pads, a problem of an no-patterned region created in an active region surrounded by an I/O region arises in a highly integrated circuit or a circuit with a small number of gates. Thus, there are challenges of solving such a problem

5   and improving the yield of a semiconductor device.

SUMMARY OF THE INVENTION

The present invention provides, as a specific means for addressing the aforementioned challenges, a semiconductor

10   device comprising on the same chip at least an I/O region where an input/output pad is formed and an active region where a plurality of circuits can be mounted, wherein a plurality of logic circuits having the same functions or different functions are mounted in the active region on the same chip.

15   In the semiconductor device thus configured, an no-patterned region having no circuit mounted therein is utilized in the active region where circuits can be mounted, and a plurality of logic circuits having functions identical to or different from those of logic circuits mounted in the

20   remaining active region is mounted in the no-patterned region. Consequently, the device can be shipped as a product if at least one of the logic circuits operates normally to significantly improve and more effectively utilize the semiconductor device.

25   In addition, when the plurality of mounted circuits are different from one other and if some of the circuits do not operate normally, the device can be delivered as an LSI having the functions of the other circuits operating normally. If all the circuits operate normally, the device can be delivered

30   as one product having different functions to provide various applications.

Furthermore, when the plurality of circuits have the

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same functions and all of them operate normally, the device can be delivered as a semiconductor product having a plurality of logic circuits with the same functions mounted thereon, and thus all the circuits can be effectively utilized with appropriate design of peripheral circuits.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagram for explaining a semiconductor chip forming part of a semiconductor device to which the present invention is applied;

Fig. 2 is a diagram for explaining two active regions formed on the semiconductor chip;

Fig. 3 is a circuit diagram showing circuits mounted on the semiconductor chip;

Fig. 4 is a circuit diagram showing a circuit for producing an SEL signal for the circuit in Fig. 3; and

Fig. 5 is a plan view showing a semiconductor chip constituting part of a conventional semiconductor device.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A semiconductor device formed with a semiconductor chip 10 shown in Fig. 1 will be described as an embodiment of the present invention. In the semiconductor chip 10, an active region 11 comprises a P-type semiconductor or N-type semiconductor substrate and this is a region where circuits can be mounted, and in addition, this region is an inside region surrounded by an I/O region 12.

Arranged in the I/O region 12 are a plurality of input/output pads 14 which are electrodes for connecting lead-out terminals for a logic LSI with a circuit inside the semiconductor chip through bonding wire. Each of the input/output pads 14 is shaped to have a square with a side

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of approximately 100 im.

A hatched portion in Fig. 1 is an no-patterned region 13 where no circuit is mounted if only one logic circuit block is mounted in the active region 11 surrounded by the I/O region 12.

Since recent LSIs have been increasingly miniaturized, higher speed processing is allowed, and an extremely large-scale integrated circuit can be realized in a very limited area on a chip, such a large no-patterned region is often created. In the example shown, the no-patterned region 13 occupies more than half of the active region 11.

As shown in Fig. 2, a portion of the no-patterned region shown in Fig. 1 is defined as a boundary region 15, and regions on both sides of the boundary region 15 are defined as a first active region 16 and a second active region 17, respectively. In the second active region 17, circuits having the same functions as or circuits having different functions from circuits mounted in the first active region 16 are mounted. It should be noted that the area of the first active region 16 may or may not be equal to the area of the second active region 17.

As shown in Fig. 3, a circuit block mounted in the first active region 16 is defined as a block A, while a circuit block mounted in the second active region 17 is defined as a block B. Each of the block A and block B may be a functional block including a plurality of circuits or a primitive cell which is the minimum unit of a circuit. The block A and block B may include circuits having the same functions or circuits having different functions from each other.

In Fig. 3, devices other then the block A and block B and signal lines form a selection circuit for operating the block A or block B and are mounted on the semiconductor chip

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The block A and block B are circuits which operate by connecting their GND terminals to the ground and their V_{dd} terminals to V_{dd}. The block A is configured such that the GND terminal is connected to the ground when an N-channel transistor T_{na} is turned on, and the V_{dd} terminal is connected to V_{dd} when a P-channel transistor T_{pa} is turned on. On the other hand, the block B is configured such that the GND terminal is connected to the ground when an N-channel transistor T_{nb} is turned on, and the V_{dd} terminal is connected to V_{dd} when a P-channel transistor T_{pb} is turned on.

As shown in Fig. 4, an SEL signal for turning on/off each transistor is a signal set on the basis of a signal input from a pad PT which is one of the plurality of input/output pads 14 shown in Figs. 1 and 2, and the signal input from the pad PT is connected to an input terminal of a buffer circuit buff. The input terminal side of the buffer circuit buff is connected to V_{dd} through a resistor R_1 and a fuse X serving as a disconnecting section, and connected to the ground through a resistor R_2 and a fuse Y serving as a disconnecting section. The disconnecting section is not limited to such fuse.

The fuse X and the fuse Y are made, for example, from tungsten or aluminum, and can be blown by a laser beam output from a laser repair apparatus. When the fuse X is blown, the SEL signal is permanently set to LOW level, and when the fuse Y is blown, the SEL signal is permanently set to HIGH level. When the fuse Y is blown, the pad PT is released. When neither of the fuse X nor the fuse Y is blown, the SEL signal is set according to the logic level of a signal input from the pad PT.

Continuing description with reference to Fig. 3, common signals are input from pads IN 1, IN2 to the block A and block

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B.   The SEL signal is connected to a gate terminal of the P-channel transistor T_{pa} and connected to a gate terminal of the N-channel transistor T_{na} through an inverter I_a for the block A, while the SEL signal is connected to a gate terminal

5   of the P-channel transistor T_{pb} through an inverter I_b and connected to a gate terminal of the N-channel transistor T_{nb} for the block B.   It should be noted that since the block A and block B are formed on the same chip and use the common substrate, the GNDs are common to both blocks and the

10   transistors T_{na}, T_{nb} may be removed if a P-type device is used.

When the SEL signal is set to LOW level, both the P-channel transistor T_{pa} and N-channel transistor T_{na} are turned on, power and ground are supplied to the block A and the circuit constituting the block A operates.   However, since both the

15   P-channel transistor T_{pb} and N-channel transistor T_{nb} are turned off, power and ground are not supplied to the block B, and the circuit constituting the block B does not operate.

At this point, as a result of the supply of the signal SEL at LOW level to control terminals of tri-state buffers

20   T_{a1}, T_{a2} connected to two output terminals A_{out1} and A_{out2} of the block A, both outputs are active (bi-state), and thus outputs from the output terminals A_{out1}, A_{out2} of the block A are output as they are to pads OUT 1, OUT 2.

On the other hand, as a result of the supply of the signal

25   SEL at LOW level to control terminals of tri-state buffers T_{b1}, T_{b2} connected to two output terminals B_{out1} and B_{out2} of the block B, both outputs are open, and thus outputs from the output terminals B_{out1}, B_{out2} of the block B are not output to the pads OUT 1, OUT 2.   In other words, when the signal SEL is set to

30   LOW level, only the functions of block A are performed as a whole.

Conversely, when the signal SEL is set to HIGH level,

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since both the P-channel transistor T_{pa} and N-channel transistor T_{na} are turned off, neither power nor ground is supplied to the block A and thus the block A does not operate. However, since both the P-channel transistor T_{pb} and N-channel

5   transistor T_{nb} are turned on, power and ground are supplied to the block B, and thus the circuits constituting the block B operates.

At this point, as a result of the supply of the signal SEL at HIGH level to the control terminals of the tri-state

10   buffers T_{a1}, T_{a2} connected to the two output terminals A_{out1} and A_{out2} of the block A, both outputs are open, and thus outputs from the output terminals A_{out1}, A_{out2} of the block A are not output to the pads OUT 1, OUT 2.

On the other hand, as a result of the supply of the signal

15   SEL at HIGH level to the control terminals of the tri-state buffers T_{b1}, T_{b2} connected to the two output terminals B_{out1} and B_{out2} of the block B, both outputs become active (bi-state), and outputs from the output terminals B_{out1}, B_{out2} of the block B are output as they are to the pads OUT 1, OUT 2. In other

20   words, when the signal SEL is set to HIGH level, only the functions of block B are performed as a whole.

In this manner, one of the two blocks can be operated and the other block can be prevented from operating only by setting the SEL signal to LOW level or HIGH level. Thus, for

25   example when the block A is found not to operate normally during a test stage, this device can be delivered as a semiconductor device in which only the block B operates by blowing the fuse Y to fix the SEL signal to HIGH level. Conversely, when the block B is found not to operate normally, this device can be

30   delivered as a semiconductor device in which only the block A operates by blowing the fuse X to fix the SEL signal to LOW level.

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In addition, when both of the block A and block B are found to operate normally, this device may be delivered with one of the blocks being operable by blowing the fuse X or the fuse Y or with both of the blocks being operable. When both of the blocks are operable, one of the block A and block B is selected by a signal input to the pad PT from an external circuit for operation.

Next, description will be made for the yield when the block A and block B have the same functions. The yield refers to the probability that the device can be delivered as a product with one or both of the two mounted circuits operating normally.

When the block A and block B have the same functions, assuming that a fraction defective of the block A is P_A and a fraction defective of the block B is P_B, the probability of the block A operating normally is $(1-P_A)$ and the probability of the block B operating normally is $(1-P_B)$. Thus, assuming that the probability of both blocks operating normally is G_{OO}, the following relational expression (1) holds:

$$G_{OO}=(1-P_A) \cdot (1-P_B) \qquad (1)$$

Also, assuming that the probability of the block A operating normally and the block B not operating normally is G_{OX}, the following relational expression holds:

$$G_{OX}=(1-P_A) \cdot P_B \qquad (2)$$

On the other hand, assuming that the probability of the block A not operating normally and the block B operating normally is G_{XO}, the following relational expression holds:

$$G_{XO}=P_A \cdot (1-P_B) \qquad (3)$$

When the block A and block B have the same functions, P_A is equal to P_B and thus the relational expressions (4), (5), and (6) hold assuming that $P_A=P_B=P$:

$$G_{OO}=(1-P)^2 \qquad (4)$$

$$G_{OX}=(1-P) \cdot P \qquad (5)$$

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$$G_{XO} = P \cdot (1-P) \tag{6}$$

Assuming that the probability of at least one of the block A and block B operating normally is G_{AB}, the following relational expression (7) holds:

$$G_{AB} = G_{OO} + G_{OX} + G_{XO} \tag{7}$$

Here, assuming that P=0.15 and when this value is substituted into the expressions (4), (5), and (6) to determine G_{OO}, G_{OX}, and G_{XO}, and the resultant values are substituted into the expression (7), G_{AB} is equal to 0.9775 (97.75%). In other words, the yield is 97.75% when the block A and block B have the same functions.

On the other hand, in a conventional semiconductor device which has only one block with a fraction defective P mounted on one semiconductor chip, the probability G of that block operating normally can be determined by using the following relational expression (8):

$$G = 1 - P \tag{8}$$

When P is equal to 0.15 similarly to the foregoing, G is equal to 0.85 (85%). Thus, when two blocks having the same functions are mounted on one semiconductor chip, the yield is improved by 12.75% (97.75-85=12.75).

Conventionally, when a circuit does not operate normally due to introduced dust, wafer crack, over-etching or under-etching in processes in manufacturing an LSI, that semiconductor device is discarded. In the present invention, however, a semiconductor device can be delivered if any one of a plurality of mounted circuits operates normally, and the yield can be significantly improved.

In addition, since an no-patterned region on a semiconductor chip can be considerably reduced to effectively utilize a semiconductor constituting a substrate, the utilization ratio for a wafer is significantly increased.

Furthermore, when a plurality of mounted blocks have different functions from one another, one kind of photo-mask can realize a plurality of functions to eliminate the need for forming a number of expensive photo-masks, which allows

5 a reduction in development cost. For a circuit block requiring exacting performance, several kinds of blocks having the same functions and formed with different mask dimensions are mounted such that an optimal block can be selected there-from according to variations in processing possibly involved in manufacturing,

10 thereby making it possible to deliver a product in which only a block having desired performance can operate. This will present a solution when an integration degree becomes higher to impose limitations on processing accuracy in the future.

In semiconductor devices such as SRAMs (Static Random

15 Access Memory) or DRAMs (Dynamic Random Access Memory), to prevent functions of the entire device from being impaired when some of memory cells are defective during manufacturing, a typical approach is to previously provide spare memory cells (redundant circuits) on a chip and to access a spare memory

20 cell instead of the defective memory cell at the time of memory access. This approach is employed to improve the yield of the semiconductor device.

When an attempt is made to improve the yield in a logic LSI with an approach similar to that for a memory element,

25 however, only a defective portion of a circuit cannot be replaced with a spare circuit as in memory cells, and a redundant circuit for supporting the entire logic circuit is required to double the chip size. This is no longer what can be called a redundant circuit, and it is thus substantially impossible

30 to provide a redundant circuit for a logic circuit. For this reason, a redundant circuit has been hardly provided for a logic LSI conventionally, and when a portion of a logic circuit

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is defective, the entire logic LSI must be discarded.

To address this, since an no-patterned region is created with an increasingly miniaturized LSI in an active region where a circuit can be mounted, the present invention effectively utilizes such a region, which conventionally has been an no-patterned region, by mounting a redundant circuit there. Therefore, even when a portion of a logic circuit is defective, the redundant circuit is caused to function similarly thereto to allow improvement in the yield of the logic LSI.

It goes without saying that while the embodiment has been described for the two blocks mounted on one semiconductor chip, the yield is also improved when three or more blocks are mounted.